REMARKS

Claims 1-5 and 7-20 are all the claims pending in the application. Claim 6 has been canceled without prejudice or disclaimer. New claims 17-20 have been added. Reconsideration and allowance of all the claims are respectfully requested in view of the following remarks.

Amendments to the Claims

Claim 1 has been amended to incorporate the features of former claim 6. In addition, the claim language has been amended in order to improve intelligibility. No new matter is added by these purely editorial amendments. Claim 6 has been cancelled without prejudice or disclaimer.

Claim 10 has been amended by removing the last step. This step has been moved into new dependent claim 20.

The amendments of claims 2-5, 7-9 and 11-16 are of a purely editorial nature.

The subject-matter of claims 17 and 18 can be derived from claim 10 as filed. Claim 19 corresponds to the second alternative of claim 7 as filed.

Claim Rejections - 35 U.S.C. § 103

The Examiner rejected claims 1-16 under §103(a) as being unpatentable over US Patent 6,847,400 to Hosier et al. (hereinafter Hosier) in view of US Patent 7,050,094 to Krymski (hereinafter Krymski).

Applicants respectfully traverse this rejection because the references fail to disclose all of the elements as set forth and arranged in the claims.

Hosier teaches a structure which, on first sight, seems to share some of the features of the presently claimed invention. In particular, Hosier teaches providing a photodiode 10, a first transistor R1 indirectly connected between the photodiode and a first potential VR1, a readout amplifier 16, a storage means CH at the input of the readout amplifier, a second transistor SH connected between the photodiode and the readout amplifier, and a third transistor R2 connected between the input of the readout amplifier and a second potential VR2. In addition, Hosier et al. teach to provide a number of additional components.

However, Hosier fails to teach or suggest providing control of the gate voltage of second transistor SH in a manner such that the photodiode current discharges the storage means in a first phase of the integration time, as claimed in current independent claims 1 and 10. In the structure of Hosier, such operation would even be absolutely impossible, as this would imply that the discharge current flows "reversely" through amplifier 15. In contrast, it appears to be a key feature of Hosier's "transfer circuit" to provide for unidirectional charge transfer, see col. 1, lines 37-65.

Hosier also fails to teach or suggest compensating for some of the current generated by the photodiode in a last phase of the integration time, as claimed in current independent claims 1 and 10, thus providing non-linear compression. In contrast, it is a key goal of Hosier's device to provide a fully linear response curve, see col. 1, lines 49-65.

Hosier therefore clearly teaches away from the presently claimed invention.

Krymski fails to cure the above-noted deficiencies in Hosier. Krymski does disclose a structure roughly facially similar to the structure of the presently claimed invention. However, the structure of Krymski is operated in a completely different manner; during integration, only capacitance C1 is discharged. Charges are transferred twice between the photodiode and the memory capacitor C2 by briefly closing switch S2, a first time after a short integration period and a second time after a long integration period, see col. 3, lines 5-19. Further, Krymski does not teach or suggest rendering the device operable in a manner such that the photodiode discharges the memory capacitor C2 in a first phase of the integration time, nor does Krymski teach or suggest compensating for some of the current generated by the photodiode in a last phase of the integration time. It may be noted that the latter goal cannot be reasonably achieved by switches only, as disclosed in Krymski.

In light of the above, Applicants respectfully request that the Examiner withdraw this rejection.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the

Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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